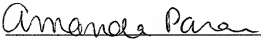


## JOINT INVENTORS

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## APPLICATION FOR UNITED STATES LETTERS PATENT

# S P E C I F I C A T I O N

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TO ALL WHOM IT MAY CONCERN:

Be it known that we, Kwang-Jun CHO, a citizen of the Republic  
of Korea, residing at San 136-1, Ami-ri, Bubal-eub, Ichon-shi, Kyoungki-do  
467-860, Republic of Korea, and Ki-Seon PARK, a citizen of the Republic of  
Korea, residing at, San 136-1, Ami-ri, Bubal-eub, Ichon-shi, Kyoungki-do 467-  
860, Republic of Korea, have invented a new and useful METHOD OF  
FORMING MEMORY DEVICE, of which the following is a specification.

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# METHOD OF FORMING MEMORY DEVICE

## BACKGROUND

### 5 Technical Field

A method for manufacturing a semiconductor integrated circuit is disclosed. More particularly, a method for manufacturing a capacitor of a semiconductor device is disclosed.

10

### Description of the Related Art

For a DRAM (Dynamic Random Access Memory), the memory cell area memorizing a bit, the standard unit for memory information, becomes smaller as the integration increases. However, the area of a capacitor cannot be reduced in proportion to the reduction of a cell. This is because more than a certain volume of capacitance is in need per cell for sensing, signal margin, sensing speed and durability for soft error caused by alpha particles. Capacitance C is in relation with the valid surface area A of a capacitor, dielectric constant  $\epsilon$  and thickness d of a dielectric substance as shown in Formula 1.

20

$$C = \epsilon A/d \quad (1)$$

Accordingly, to maintain the capacitance C of a capacitor in limited cell area, one should either reduce the thickness d of a dielectric substance, increase the valid surface area A of the capacitor, or use a material with a high dielectric constant  $\epsilon$ .

25

Among them, the methods of minimizing the thickness d of a dielectric substance and of increasing the valid surface area of a capacitor with a three dimensional structure, such as a simple stack structure, concave structure, cylindrical structure and multi-layer pin

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structure have reached their limits due to the ultra miniaturization of semiconductor manufacturing process.

A conventional dielectric layer used for a capacitor has been mainly a NO (Nitride-Oxide) or ONO (Oxide-Nitride-Oxide) thin layer. However, the current situation requires the introduction of a new material, because there is limit to increase the capacitance that is already high, even though the thickness of a dielectric substance thin layer is reduced or the surface area is increased. This is because the dielectric constant of  $\text{SiO}_2$ , NO (Nitride-Oxide) or ONO (Oxide-Nitride-Oxide) layer are small.

Accordingly, high dielectric layers, e.g.,  $(\text{Ba}, \text{Sr})\text{TiO}_3$  (BST),  $\text{SrTiO}_3$  (STO),  $(\text{Pb}, \text{Zr})\text{TiO}_3$  (PZT),  $(\text{Pb}, \text{La}) (\text{Zr}, \text{Ti})\text{O}_3$  (PLZT),  $\text{SrBi}_2\text{Ta}_2\text{O}_9$  (SBT), TaON and  $\text{Ta}_2\text{O}_5$  are introduced to substitute the conventional dielectric thin layer in a highly integrated DRAM.

For capacitors using high dielectric layers, it is difficult to use polysilicon as an electrode material. Instead, they use noble metals or their oxides, such as Pt, Ir, Ru,  $\text{RuO}_2$  and  $\text{IrO}_2$ , or conductive compounds like TiN.

For example, in case of using  $\text{Ta}_2\text{O}_5$  as a dielectric layer, MIS (Metal/Insulator/Silicon) structure or MIM (Metal/Insulator/Metal) structure should be adopted. In case of using BST, the MIM (Metal/Insulator/Metal) structure is to be employed. When forming a capacitor electrode with the metals shown above, a barrier layer of TiN, TaN, TiSiN and TaAlN should be formed necessarily to prevent the reaction between the polysilicon plug or substrate silicon and the metal, to secure the ohmic contact property, and to prevent the diffusion of oxygen,

which is used as a source while a dielectric layer is deposited.

Fig. 1 is a cross-sectional view illustrating a conventional concave capacitor.

5 A concave capacitor and a cylinder capacitor are contrived to avoid the difficulty in etching that is caused as the height of the bottom electrode increases, in a three dimensional stack capacitor in response to the high integration tendency of a DRAM. The concave or  
10 cylinder capacity makes it possible to avoid the difficulty in etching process and control the height of a storage node.

Fig. 2 is a cross-sectional view depicting a conventional stack capacitor.

15 The stack structure is formed as follows. First, after the formation of a inter-layer insulation film 305 on a semiconductor substrate 300, a storage contact hole is formed and connected to an active region (not illustrated) of the semiconductor substrate through the  
20 inter-layer insulation film. Subsequently, a plug is molded by forming a polysilicon 310, silicide layer 315, and barrier layer 320 respectively. After the formation of the plug, the bottom electrode is deposited, etched selectively and thus a bottom electrode pattern 325 is  
25 formed. A stack capacitor is formed by molding a dielectric layer 330 and a top electrode 335 on the bottom electrode pattern 325 and patterning it.

When molding the bottom electrode of a simple stack capacitor with the metal as described above, there are  
30 following problems. That is, after the deposition of a metallic layer which forms the bottom electrode in the CVD (Chemical Vapor Deposition), the substrate should be etched and patterned. However, the noble metals used as a

bottom electrode are hard and stable they hardly react with other chemicals, which makes them difficult to etch. It may be possible to do patterning in the reactive ion etching (RIE), but it is still difficult to obtain a  
5 desired sidewall profile with currently available etching equipment. Also, it is difficult as well to get a material for an etching mask with a lower etching degree than the noble metals. Lastly, the metallic layer deposited in the CVD has a problem that the amount of leakage  
10 current increases. This is because the surface of an electrode becomes rough by the elimination of impurities and subsequent thermal treatment, and thus the dielectric layer is not formed with a nonuniform thickness.

15 **SUMMARY OF THE DISCLOSURE**

Therefore, a method for manufacturing a semiconductor device is disclosed in which a capacitor can be formed with a simplified process.

20 A method for manufacturing a semiconductor device is also disclosed in which a metallic bottom electrode can be formed in a capacitor without etching a metallic layer.

A method for manufacturing a semiconductor device is also disclosed which can suppress the generation of leakage current caused by the rough surface of a bottom  
25 electrode.

In an embodiment of the disclosed method, a method for manufacturing a semiconductor device comprises: a) forming a contact hole to expose the joining portion by etching an inter-layer insulation layer on top of a  
30 semiconductor substrate optionally; b) forming a contact plug inside the contact hole; c) molding an etch stop layer and a sacrificial oxide layer on the contact plug and the inter-layer insulation layer; d) molding a

storage node hole to expose the contact plug by etching the etch stop layer and the sacrificial oxide layer optionally; e) forming a TiN bottom electrode inside the storage node hole in the CVD method; f) separating the  
5 TiN bottom electrode neighboring the sacrificial layer by removing the TiN layer thereon; g) exposing the TiN bottom electrode pattern by removing the sacrificial oxide layer; h) forming a dielectric layer on the TiN bottom electrode pattern; and molding a top electrode on  
10 the dielectric layer.

#### **BRIEF DESCRIPTION OF THE DRAWINGS**

The above and other features of the disclosed method will become apparent from the following description of  
15 the preferred embodiments given in conjunction with the accompanying drawings, wherein:

Fig. 1 is a cross-sectional view illustrating a conventional concave capacitor;

Fig. 2 is a cross-sectional view depicting a  
20 conventional stack capacitor; and

Figs. 3A to 3G are cross-sectional views showing the process for forming a capacitor of a semiconductor device in accordance with one disclosed embodiment.

#### **DETAILED DESCRIPTION OF THE PRESENTLY PREFERRED EMBODIMENTS**

Other aspects of the disclosed methods will become apparent from the following description of the  
embodiments with reference to the accompanying drawings,  
30 Figs. 3A to 3G, which is set forth hereinafter.

First, as shown in Fig. 3A, an element separation layer 105 is formed on a predetermined domain of a semiconductor substrate 100 to define active domains and

inactive domains, and a MOS transistor composed of a gate insulation layer 110, gate electrode 115 and source/drain joining domain 120 is molded on the semiconductor substrate 100. Although not illustrated in the drawing, a  
5 spacer may be formed on the side of the gate electrode 115. A first contact hole is molded to expose the joining domain 120 of the MOS transistor to be linked to a bitline by forming a first inter-layer insulation layer 125 on the front of the semiconductor substrate formed  
10 with the MOS transistor and patterning it. Then, a bitline 130 that is connected to the joining domain 120 is formed inside the first contact hole. Subsequently, a second inter-layer insulation layer 135 is molded on the front side of the semiconductor substrate 100 formed with  
15 the bitline 130. A second contact hole is molded by optionally etching the first and the second insulation layers 125, 135 to expose the joining domain 120 of the MOS transistor connected to a capacitor. A polysilicon plug 145 is molded inside the second contact hole by  
20 depositing polysilicon to fill up the second contact hole on the front side of the semiconductor substrate 100 formed with the second contact hole and etching the polysilicon until the second inter-layer insulation layer 135 is exposed.

25 As illustrated in Fig. 3B, an etch stop layer 150 and a sacrificial oxide layer 155 are molded on top of the semiconductor substrate 100 where the polysilicon plug 145 are formed. The etch stop layer 150 is formed of  $\text{SiN}$ ,  $\text{Al}_2\text{O}_3$ ,  $\text{SiON}$  or  $\text{Si}_3\text{N}_4$ , which has a high wet etch  
30 selection rate to the upper layer, the sacrificial oxide layer 155.

As depicted in Fig. 3C, a storage node hole 160 is molded to expose the polysilicon plug 145 and the inter-

layer insulation layer 135 around it by dry-etching the sacrificial oxide layer 155 and the etch stop layer 150 optionally and forming a sacrificial oxide layer pattern 155A and an etch stop layer pattern 150A.

5 As shown in Fig. 3D, a silicide layer 165 is molded to reduce contact resistance by forming an ohmic contact on the surface of the polysilicon plug 145 exposed on the bottom surface of the storage node hole 160. The procedures for forming the silicide layer 165 are  
10 described hereinafter. Forming a metallic layer by depositing Ti, Co or Ni in the CVD method, it goes through a thermal treatment by using the rapid thermal processing (RTP) or a furnace. In the thermal treatment, the metallic layer part contacting the inter-layer  
15 insulation layer 135 or sacrificial oxide layer pattern 155A doesn't show a silicide reaction. However, the metallic layer on the polysilicon plug 145 reacts to the polysilicon plug 145 and becomes a silicide, thereby forming  $\text{TiSi}_2$ ,  $\text{CoSi}_2$  or  $\text{NiSi}_2$  silicide layer 165 on the  
20 surface of the polysilicon plug 145. Cleaning the thermally treated semiconductor substrate with a mixture of  $\text{H}_2\text{SO}_4$  and  $\text{H}_2\text{O}_2$ , the metallic layer that remains on the inter-layer insulation layer or sacrificial pattern 155A is removed.

25 Subsequently, a TiN bottom electrode pattern 170 is molded by embedding TiN in the storage node hole 160 in the CVD method and performing a storage node separation on the conductor layer of the bottom electrode. The storage node separation is to separate a plurality of TiN  
30 bottom electrode pattern 170 by removing TiN until the upper surface of the sacrificial oxide layer is exposed in the etch back or chemical-mechanical polishing (CMP) method.



Conventionally, a barrier layer made of TiN or others is formed on the silicide layer to prevent the oxygen diffusion after forming the silicide layer 165. However, the disclosed method skips the procedure of forming a barrier layer as mentioned before and simplifies the process by forming the entire bottom electrode with TiN.

Subsequently, the sacrificial oxide layer 155A is wet etched and removed, and as shown in Fig. 3E, a TiN bottom electrode pattern 170 of a simple stack structure is exposed.

Then, as illustrated in Fig. 3F, a dielectric layer 175 and an top electrode 180 are molded one by one on the TiN bottom electrode pattern 170.

The dielectric layer 175 is formed of BST, STO, PZT, PLZT, SBT, TaON or Ta<sub>2</sub>O<sub>5</sub>, and for the top electrode 180, such an oxide electrode as TiN, Ru, Pt, Ir, Os, W, Mo, Co, Ni, Au, Ag, RuO<sub>2</sub> or IrO<sub>2</sub> can be used.

The disclosed method simplifies the process of manufacturing a semiconductor by omitting the procedures for forming a barrier layer on the conventional polysilicon contact plug.

Also, it is possible to form a bottom electrode without carrying out the process of etching a metallic layer for patterning and the deterioration of electric properties by leakage current can be prevented, because a TiN bottom electrode with little surface roughness can be obtained from the smooth sacrificial interface.

While the present invention has been described with respect to certain preferred embodiments, it will be apparent to those skilled in the art that various changes and modifications may be made without departing from the scope of the invention as defined in the following claims.